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UNCERTAINTY IN TESTING OF OPEN CIRCUIT SUPPLY FAULTS IN CMOS LOGIC CIRCUITS

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Abstract: This kind of fault is represented by a break in a power supply track of a CMOS integrated circuit. In circuits containing such faults, current can be supplied through the substrate of integrated circuit and logic gates can operate normally, with insignificant changes in their performance parameters. For this reason, the fault may not be detected by any form of conventional testing. The results of our PSPICE simulations are in accordance with the measurements on real circuits containing such faults. A faulty circuit may be susceptible to latch-up behaviour and may fail in this way. Transient latch-up testing is a possibility to detect such faults, but a degree of uncertainty always remains.

Keywords: CMOS logic, Open circuit supply faults, Stuck-open fault, Latch-up.

1. INTRODUCTION

The stuck-at, bridging and stuck-open faults in CMOS circuits, and some methods for their detection, were studied in literature (Abraham and Fuchs, 1986; Bate and Miller, 1988).

A special case of the stuck-open fault arises when the open circuit defect occurs in one of the supply tracks. In this case the tracks or contacts to one of the power supplies for a logic gate become open circuit, that is very high resistance. The most probable cause of the fault is a photolithographic defect in a conducting layer, but the fault may also occur during the operating life of the IC due to electromigration failure in tracks or contacts. These faults are of increasing concern with modern submicron CMOS technologies used in our days (Johnson and Morant, 1996).

Two examples of defects which cause open circuit faults in the Vss supply line are given in fig.1, but the effects of them are quite distinct. For the fault *a*, the defect has occurred in the track which is providing the Vss supply to the output inverter.
The transistors of this cell remain connected to the local substrate contact for the gate and current may flow through the substrate contact to or from the logic gate (see fig. 2). For the case of defect *b*, the output inverter of the cell is essentially isolated from

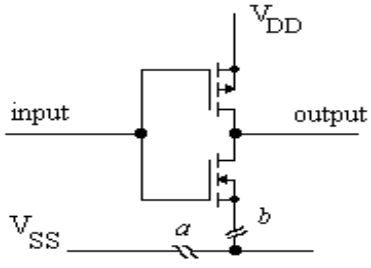

Fig. 1. Two quite distinct open circuit faults which may isolate a CMOS inverter output from the Vss supply.

the Vss supply. This is the conventional model of an open circuit supply fault and the detection of this kind of fault is a simple problem.

2. ANALYSIS OF THE *a* TYPE OPEN CIRCUIT SUPPLY FAULT

(Johnson and Morant, 1996) showed that the fault arising from type *a* defects is more common than complete isolation of transistors from a supply. Fig. 2 illustrates the both types of faults in a partial cross-section of a CMOS inverter. In the case of *a* type fault, when the n-channel transistor which is apparently isolated from the Vss supply is switched on, the current may flow through the substrate *p*-resistance. Measurements on the test circuits indicated a value of 450Ω for a single gate in 3 μm *p*-well CMOS technology, and this resistance is found to be independent of the distance between the faulty gate and the fault free substrate contact which is acting as the power supply for the gate (Johnson and Morant, 1996). In the case of *b* type fault, when the *n*-channel transistor is switched on, the current cannot flow through substrate because of a *p-n* junction inverse biased. The resistance between source and Vss track become enormous and the output of the inverter will be stuck-at logic 1.

2.1. Simulations for "a" type open circuit supply faults

The break in the power supply which generates the *a* type fault has the effect of adding a series resistor between the *n*-channel pull-down network and the Vss supply. This has no effect on the DC or logical operation of the gate, but the propagation delay of the gate is increased. The model for PSPICE simulations is presented in fig. 3. The transistors parameters W and L, and the common value of resistance Rs are those indicated in (Johnson and Morant, 1996) for a 3 μm p-well CMOS technology. These values are the following: Wp = 20 μm, Lp = 3 μm, Wn = 8 μm, Ln = 3 μm, Rs = 450 Ω. Load

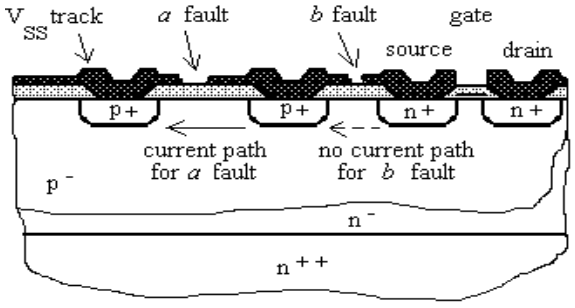

Fig. 2. Cross-section of a CMOS inverter with open circuit supply faults in the Vss supply.

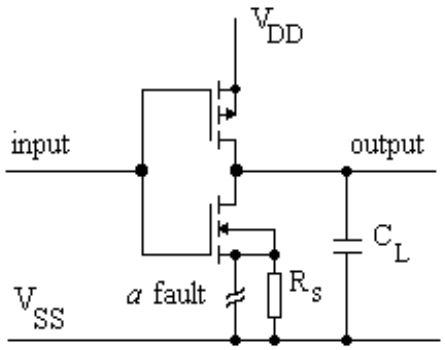

Fig. 3. PSPICE simulation model of a CMOS inverter with an *a* type fault in the Vss supply.

capacitor CL has two distinct values in our simulations: one of 50 fF, if the inverter is an internal gate of the IC, and one of 50 pF, the maximum capacitive test load indicated in (Philips Semiconductors B. V., 1991) that guarantees the published a.c. characteristics of a HCMOS IC, if the inverter is an output gate of the IC.

As it was expected from the CMOS theory, the presence of the substrate resistance don't affect the DC characteristics of the faulty gate. They are the same as a fault free gate with the logic function unaffected by the presence of the fault.

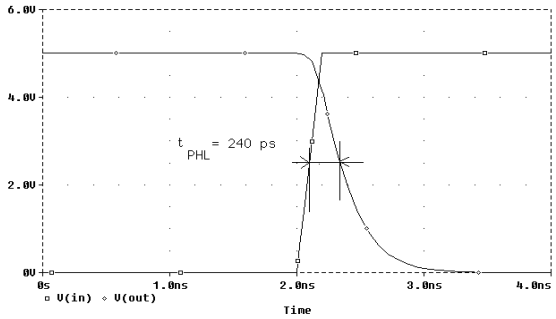

Fig. 4. Propagation delay of a fault free CMOS inverter loaded with 50 fF.

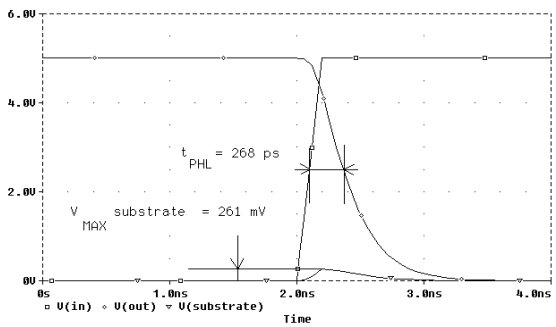

Fig. 5. Propagation delay and the maximum substrate voltage of a faulty CMOS inverter loaded with 50 fF.

Dynamic operation of a fault free inverter loaded with 50 fF is represented in fig. 4, and the operation of the same faulty inverter is represented in fig. 5. The propagation delay is defined as the time between the specified reference points (50% on the input and output waveforms), with the output changing from the defined HIGH level to the defined LOW level (Philips Semiconductors B. V., 1991). The difference in the propagation delays, defined as the times between the two gates is negligible (about 30 ps) and the transient response of the gate is practical unaffected by the presence of the fault. The only modification is the raising of the substrate potential during the transition, up to a maximum value of 261mV, as may be seen in fig. 5. This increase in the substrate potential due to supply current flow during transitions has two unwanted consequences: a lowered threshold voltage of the *n*- channel transistors in the faulty gates during transitions, and a greater probability of inducing latch-up in the CMOS circuit.

The figures 6 and 7 represents the results of a transient simulation of fault free and respectively stuck-open supply CMOS inverters, both with a capacitive load of 50 pF. The propagation delay, defined as above, is about 30 ns, a value that can be

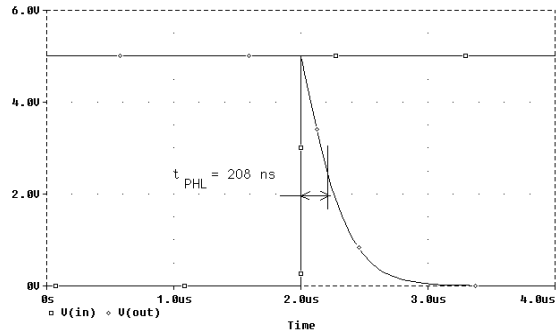

Fig. 6. Propagation delay of a fault free CMOS inverter loaded with 50 pF.

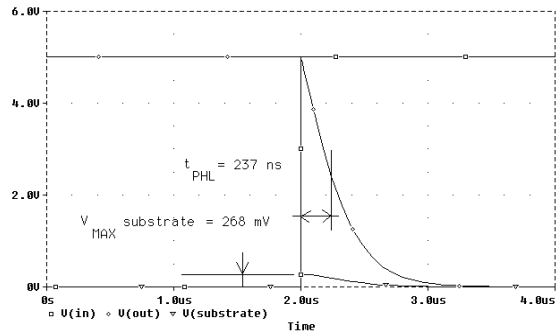

Fig. 7. Propagation delay and the maximum substrate voltage of a faulty CMOS inverter loaded with 50 pF.

measured, but in relative terms, the results are the same with those obtained in previous simulation (fig. 4 and fig. 5). Only the increase of substrate potential is greater than in previous case and the maximum value obtained is 268 mV.

2.2. Susceptibility to latch-up

Latch-up is a particular problem to CMOS devices. Fig. 8 shows a simplified cross-section of a CMOS inverter and the structure of the parasitic bipolar transistors. This transistors generate a structure of parasitic thyristor which can induces latch-up. When a negative voltage is applied on input terminal, T4 is turned on. The current flow from power supply through Rn turns on the transistor T1. When T1 becomes conductive, current flows from power supply through Rp, by which T2 is put into conduction, too. Then, as the base of T2 is rebiased by collector current from T1, the closed loop consisting of T1 and T2 reacts. The presence of Rs resistance increases the probability of latch-up. Latch-up occurs by positive pulse, too.

The probability of latch-up occurring due to the rise in substrate potential will depend on the local circuit layout. Measurements taken on the test circuits previously described indicate that the substrate potential must rise generally by more than 190 mV before latch-up is induced in the circuit (Johnson and Morant, 1996). Our simulations indicate a greater value of substrate potential and, in this case, a test for latch-up during circuit transitions may be applied.

A good thing for digital systems designers, but not so good for our intention to generate a test for CMOS IC's based on latch-up, is the fact that most of the IC's manufacturers are trying to improve latch-up immunity of their products. Hitachi provides enough guard band by applying diffusion layer around inputs and outputs, taking care not to connect input to *p*+ diffusion layer. Input voltage for

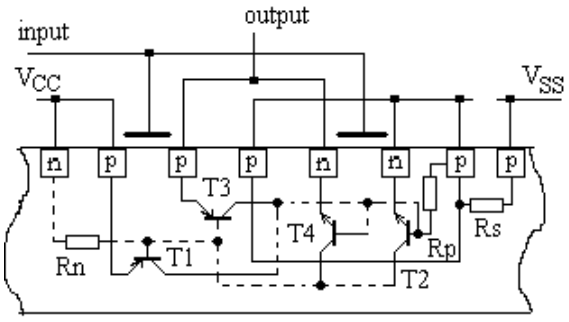

Fig. 8. Simplified cross-section structure of CMOS inverter.

16K static RAM memory HM6116, for example, is specified as follows (Hitachi Europe Ltd., 1995):

$V_{IH\ MAX}$ = 6,0 V (not depending on V_{CC})
$V_{IL\ MIN}$ = - 3,0 V (pulse width = 50 ns)
= - 0,3 V (DC level)

This mechanism of latch-up is not already the same, and we can talk about latch-up only in probabilistic terms. The current flowing through substrate may be greater than that simulated for a number of reasons (multiple faults, local circuit layout, load capacitance). It is possible that the open circuit supply fault may induce latch-up in some circumstances, but many such faults may arise for which latch-up will not occur.

3. CONCLUSIONS

We saw that the open circuit supply fault may not produce a stuck-at or stuck-open fault effect and classical test patterns will not detect such failures. Recently, a new test method based on the measurement of the quiescent supply current of the IC was proposed for a great number of faults in CMOS logic (Novellino, 1995) but, unfortunately, the open circuit supply fault does not increase the quiescent supply current and that test will not reveal the fault. A delay fault testing will not point this kind of fault, because, like PSPICE simulations show, the fault does not significantly increase the propagation delay of the gates. A greater value of the load capacitor increases the propagation delay, but the difference between the two times of propagation is the same, in relatively terms.

It seems that the only effect that may occur is that the faulty circuit can go into latch-up, in spite of the uncertainty in the function of this mechanism. In conclusion, the only form of test that can be potentially detect this kind of fault seems to be testing for latch-up during transitions of the circuit gates. On the basis of our results in simulation, we recommend a toggle test for latch-up at maximal nominal supply voltage, with all output gates of the circuit loaded with at least 50 pF, or even a greater value. This condition maximizes the increase of substrate voltage during transitions and, in the same time, the probability of latch-up occuring.

The early detecting of this kind of fault is important because exists the possibility that latch-up may occur under certain operating conditions in the field of the user. The continuous improvement of latch-up immunity of IC's is approving for a good functioning of a digital system in the field of the user, even if this kind of fault exists, but from another point of view, this fact increases the degree of uncertainty in latch-up testing of CMOS circuits.

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