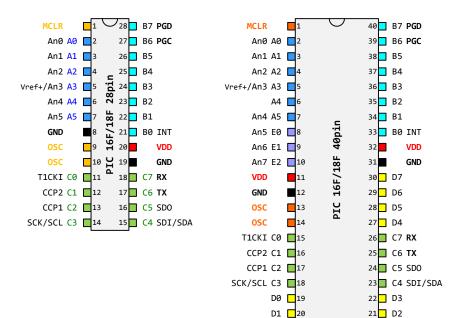
## PIC hardware quick reference



## Hardware:

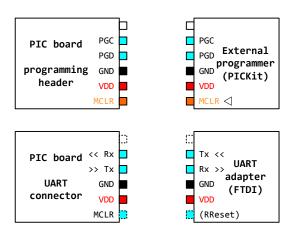
- Place quartz (and corresponding capacitors) as close as possible to the pins.
- Place 100n capacitor as close as possible to supply pins. It can be any value close to that; use the smallest footprint available
- If you have room it's better to provide a programming header (see drawing).
- The advantage of having the UART connector as pictured is that the board can be powered from a PicKit programmer.

## Software:

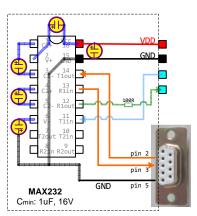
Thing to be aware of (depending on PIC type):

A4 may be open collector (cannot drive)

- Ax pins may start as Analog
- Bx pins may start as Analog



- The pins that are white or dotted are not necessary, but useful when inserting the connector (to have same number of pins).
- Rx and Tx signals are relative to the corresponding device and usually connected Rx from one with Tx from another: it is better to mark them with arrows indicating the direction of the transmission.



• The small resistor is optional.

If you turn it around you will see that is pin compatible with the connector on the left

irect addr. (1)	00h	Indirect addr. (1)	80h	Indirect addr. (1)	100h	Indirect addr. (1)
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG
PCL	02h	PCL	82h	PCL	102h	PCL
STATUS	03h	STATUS	83h	STATUS	103h	STATUS
FSR	04h	FSR	84h	FSR	104h	FSR
PORTA	05h	TRISA	85h	WDTCON	105h	SRCON
PORTB	06h	TRISB	86h	PORTB	106h	TRISB
PORTC	07h	TRISC	87h	CM1CON0	107h	BAUDCTL
PORTD <sup>(2)</sup>	08h	TRISD <sup>(2)</sup>	88h	CM2CON0	108h	ANSEL
PORTE	09h	TRISE	89h	CM2CON1	109h	ANSELH
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON
PIR1	0Ch	PIE1	8Ch	EEDAT	10Ch	EECON1
PIR2	0Dh	PIE2	8Dh	EEADR	10Dh	EECON2 <sup>(1)</sup>
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved
TMR1H	0Fh	OSCCON	8Fh	EEADRH	10Fh	Reserved
T1CON	10h	OSCTUNE	90h		110h	
TMR2	11h	SSPCON2	91h		111h	
T2CON	12h	PR2	92h		112h	
SSPBUF	13h	SSPADD	93h		113h	
SSPCON	14h	SSPSTAT	94h		114h	
CCPR1L	15h	WPUB	95h		115h	
CCPR1H	16h	IOCB	96h	General	116h	General
CCP1CON	17h	VRCON	97h	Purpose Registers	117h	Purpose Registers
RCSTA	18h	TXSTA	98h	Registers	118h	Registers
TXREG	19h	SPBRG	99h	16 Bytes	119h	16 Bytes
RCREG	1Ah	SPBRGH	9Ah		11Ah	
CCPR2L	1Bh	PWM1CON	9Bh		11Bh	
CCPR2H	1Ch	ECCPAS	9Ch		11Ch	
CCP2CON	1Dh	PSTRCON	9Dh		11Dh	
ADRESH	1Eh	ADRESL	9Eh		11Eh	
ADCON0	1Fh	ADCON1	9Fh		11Fh	
General	20h 3Fh	General Purpose Registers	A0h	General Purpose	120h	General Purpose
Purpose Registers	40h	80 Bytes		Registers 80 Bytes		Registers 80 Bytes
96 Bytes	6Fh		EFh		16Fh	
-	70h 7Fh	accesses 70h-7Fh	F0h FFh	accesses 70h-7Fh	170h 17Fh	accesses 70h-7Fh
Bank 0		Bank 1		Bank 2		Bank 3

Mnemonic,		Description	Cycles		14-Bit	Opcode	9	Status	
Opera	nds	Description		MSb			LSb	Affected	Notes
		BYTE-ORIENTED FILE REGI	STER OPE	RATIO	NS				
ADDWF	f, d	Add W and f	1	0.0	0111	dfff	ffff	C, DC, Z	1, 2
ANDWF	f. d	AND W with f	1	00	0101	dfff	ffff	z	1, 2
CLRF	f	Clear f	1	00	0001	lfff	ffff	z	2
CLRW	-	Clear W	1	0.0	0001	0xxx	XXXX	Z	
COMF	f. d	Complement f	1	00	1001	dfff	ffff	z	1, 2
DECF	f, d	Decrement f	1 1	00	0011	dfff	ffff	z	1, 2
DECFSZ	f. d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1, 2, 3
INCF	f, d	Increment f	1	0.0	1010		ffff	Z	1, 2
INCESZ	f. d	Increment f. Skip if 0	1(2)	0.0	1111			_	1, 2, 3
IORWF	f. d	Inclusive OR W with f	1	00	0100		ffff	z	1, 2
MOVE	f, d	Move f	1	00	1000	dfff	ffff	7	1, 2
MOVWE	f	Move W to f	1 1	0.0	0000		ffff	_	.,_
NOP		No Operation	l i	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	l i	0.0	1101		ffff	С	1, 2
RRF	f. d	Rotate Right f through Carry	i	00	1100		ffff	Č	1, 2
SUBWF	f, d	Subtract W from f	1 1	00	0010		ffff	C. DC. Z	1, 2
SWAPF	f. d	Swap nibbles in f	l i	00	1110		ffff	0, 00, 2	1, 2
XORWF	f, d	Exclusive OR W with f	i	00	0110		ffff	z	1, 2
,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	., .	BIT-ORIENTED FILE REGIS	TER OPER						.,.
DOE		Bit Clear f							4.0
BCF BSF	f, b	Bit Clear t	1 1	01		bfff			1, 2
	f, b		1 .	01		bfff			1, 2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01		bfff			3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
		LITERAL AND CONTROL	OPERAT	IONS					
ADDLW	k	Add literal and W	1	11		kkkk		C, DC, Z	
ANDLW	k	AND literal with W	1	11		kkkk		Z	
CALL	k	Call Subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	_	Clear Watchdog Timer	1	0.0	0000	0110	0100	TO, PD	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	0.0	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into Standby mode	1	00	0000	0110	0011	TO, PD	
SUBLW	k	Subtract w from literal	1	11	110x	kkkk	kkkk	C, DC, Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0				
Bank	0												
00h	INDF	Addressing	this location	uses contan	te of ESR to	address data	memory (no	t a nhveical i	ragietar)				
01h	TMR0		Addressing this location uses contents of FSR to address data memory (not a physical register)  Timer0 Module Register										
02h	PCL		Program Counter's (PC) Least Significant Byte										
	STATUS	-											
03h	FSR												
04h	PORTA(3)		Indirect Data Memory Address Pointer										
05h	PORTA(3)	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0				
06h		RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0				
07h	PORTC(3)	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0				
08h	PORTD(3,4)	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0				
09h	PORTE <sup>(3)</sup>	_	_	_		RE3	RE2 <sup>(4)</sup>	RE1 <sup>(4)</sup>	RE0 <sup>(4)</sup>				
0Ah	PCLATH	_	_	_		for upper 5							
0Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF <sup>(1)</sup>				
0Ch	PIR1	_	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF				
0Dh	PIR2	OSFIF	C2IF	C1IF	EEIF	BCLIF	ULPWUIF	_	CCP2IF				
0Eh	TMR1L	Holding Re	gister for the	Least Signifi	cant Byte of	the 16-bit TM	IR1 Register						
0Fh	TMR1H	Holding Re	gister for the	Most Signific	ant Byte of t	he 16-bit TMI	R1 Register						
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T10SCEN	T1SYNC	TMR1CS	TMR10N				
11h	TMR2	Timer2 Mod	dule Register										
12h	T2CON	_	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0				
13h	SSPBUF	Synchronou	ıs Serial Por	t Receive Bu	ffer/Transmit	Register			•				
14h	SSPCON(2)	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0				
15h	CCPR1L	Capture/Co	mpare/PWM	Register 1 L	ow Byte (LSI	B)							
16h	CCPR1H	Capture/Co	mpare/PWM	Register 1 H	ligh Byte (MS	SB)							
17h	CCP1CON	P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0				
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D				
19h	TXREG	EUSART T	ransmit Data	Register									
1Ah	RCREG	EUSART R	eceive Data	Register									
1Bh	CCPR2L	Capture/Co	mpare/PWM	Register 2 L	ow Byte (LSI	B)							
1Ch	CCPR2H	Capture/Co	mpare/PWM	Register 2 H	ligh Byte (MS	SB)							
1Dh	CCP2CON	_	_	DC2B1	DC2B0	ССР2М3	CCP2M2	CCP2M1	CCP2M0				
1Eh	ADRESH	A/D Result	Register Hig	h Byte									
1Fh	ADCOND	ADCS1	ADCS0	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON				

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0					
Bank 1														
80h	INDF	Addressing	this location	uses conter	nts of FSR to	address dat	a memory (n	ot a physica	register)					
81h	OPTION_REG	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0					
82h	PCL	Program Co	Program Counter's (PC) Least Significant Byte											
83h	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С					
84h	FSR	Indirect Dat	ndirect Data Memory Address Pointer											
85h	TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0					
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0					
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0					
88h	TRISD <sup>(3)</sup>	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0					
89h	TRISE	_	_	_	_	TRISE3	TRISE2(3)	TRISE1(3)	TRISE0(3					
8Ah	PCLATH	_	_	_	Write Buffer	for the uppe	er 5 bits of th	e Program (	Counter					
8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF <sup>(1)</sup>					
8Ch	PIE1	_	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE					
8Dh	PIE2	OSFIE	C2IE	C1IE	EEIE	BCLIE	ULPWUIE	_	CCP2IE					
8Eh	PCON	_	_	ULPWUE	SBOREN	_	_	POR	BOR					
8Fh	OSCCON	_	IRCF2	IRCF1	IRCF0	OSTS	HTS	LTS	SCS					
90h	OSCTUNE	_	_	_	TUN4	TUN3	TUN2	TUN1	TUN0					
91h	SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN					
92h	PR2	Timer2 Peri	od Register											
93h	SSPADD(2)	Synchronou	ıs Serial Por	t (I <sup>2</sup> C mode)	Address Re	gister								
93h	SSPMSK <sup>(2)</sup>	MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0					
94h	SSPSTAT	SMP	CKE	D/A	Р	S	R/₩	UA	BF					
95h	WPUB	WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0					
96h	IOCB	IOCB7	IOCB6	IOCB5	IOCB4	IOCB3	IOCB2	IOCB1	IOCB0					
97h	VRCON	VREN	VROE	VRR	VRSS	VR3	VR2	VR1	VR0					
98h	TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D					
99h	SPBRG	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0					
9Ah	SPBRGH	BRG15	BRG14	BRG13	BRG12	BRG11	BRG10	BRG9	BRG8					
9Bh	PWM1CON	PRSEN	PDC6	PDC5	PDC4	PDC3	PDC2	PDC1	PDC0					
9Ch	ECCPAS	ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0					
9Dh	PSTRCON	_	_	_	STRSYNC	STRD	STRC	STRB	STRA					
9Eh	ADRESL	A/D Result	Register Lov	v Byte										
9Fh	ADCON1	ADFM	_	VCFG1	VCFG0	_	_	_	_					

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0						
Bank	Bank 2														
100h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)													
101h	TMR0	Timer0 Mo	Timer0 Module Register												
102h	PCL	Program C	ounter's (PC	) Least Sign	ificant Byte										
103h	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С						
104h	FSR	Indirect Da	ta Memory A	ddress Poin	ter										
105h	WDTCON	_	_	_	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN						
106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0						
107h	CM1CON0	C10N	C10UT	C1OE	C1POL	_	C1R	C1CH1	C1CH0						
108h	CM2CON0	C2ON	C2OUT	C20E	C2POL	_	C2R	C2CH1	C2CH0						
109h	CM2CON1	MC10UT	MC2OUT	C1RSEL	C2RSEL	_	_	T1GSS	C2SYNC						
10Ah	PCLATH	_	-	_	Write Buff	er for the up	per 5 bits of t	he Program	Counter						
10Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF <sup>(1)</sup>						
10Ch	EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0						
10Dh	EEADR	EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0						
10Eh	EEDATH	_	_	EEDATH5	EEDATH4	EEDATH3	EEDATH2	EEDATH1	EEDATH0						
10Fh	EEADRH	_	_	_	EEADRH4 <sup>(2)</sup>	EEADRH3	EEADRH2	EEADRH1	EEADRH0						

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0					
Bank 3	Bank 3													
180h	INDF	Addressing	Addressing this location uses contents of FSR to address data memory (not a physical register)											
181h	OPTION_REG	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0					
182h	PCL	Program C	ounter's (PC	) Least Sigr	ificant Byte									
183h	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С					
184h	FSR	Indirect Da	Indirect Data Memory Address Pointer											
185h	SRCON	SR1	SR0	C1SEN	C2REN	PULSS	PULSR	_	FVREN					
186h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0					
187h	BAUDCTL	ABDOVF	RCIDL	_	SCKP	BRG16	-	WUE	ABDEN					
188h	ANSEL	ANS7 <sup>(2)</sup>	ANS6 <sup>(2)</sup>	ANS5 <sup>(2)</sup>	ANS4	ANS3	ANS2	ANS1	ANS0					
189h	ANSELH	_	_	ANS13	ANS12	ANS11	ANS10	ANS9	ANS8					
18Ah	PCLATH	_	_	_	Write Buffe	r for the upp	er 5 bits of t	he Program	Counter					
18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF <sup>(1)</sup>					
18Ch	EECON1	EEPGD	_	_	_	WRERR	WREN	WR	RD					
18Dh	EECON2	EEPROM (	Control Regi	ster 2 (not a	physical reg	gister)		•	•					

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0				
TOSU		_	-	Top-of-Stack	Upper Byte (T	OS<20:16>)						
TOSH TOSL	Top-of-Stack, High Byte (TOS<15:8>) Top-of-Stack, Low Byte (TOS<7:0>)											
STKPTR		STKUNF(6)	_	SP4	SP3	SP2	SP1	SP0				
PCLATU PCLATH	— Holding Regis	ster for PC<15		Holding Regis	ster for PC<20	:16>						
PCL	PC, Low Byte											
TBLPTRU TBLPTRH	— Drogram Mar	— Table Dei	bit 21	Program Men (TBLPTR<15		nter Upper By	te (TBLPTR<20	):16>)				
TBLPTRL				(TBLPTR<7:0								
TABLAT	Program Memory Table Latch Product Register High Byte											
PRODH PRODL	Product Regi											
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF				
INTCON2 INTCON3	RBPU INT2IP	INTEDG0 INT1IP	INTEDG1	INTEDG2 INT2IE	 INT1IE	TMR0IP	INT2IF	RBIP INT1IF				
INDF0			ddress data n			changed (not	a physical regis					
POSTINCO	Uses content	s of FSR0 to a	ddress data n	nemory – value	of FSR0 pos	t-incremented	(not a physical	register)				
POSTDECO PREINCO							d (not a physica not a physical r					
PLUSW0		s of FSR0 to a					not a physical r					
FSR0H	—	—	_	_	Indirect Data	Memory Addr	ess Pointer 0, H	ligh Byte				
FSR0L WREG	Indirect Data Working Regi	Memory Addr	ess Pointer 0,	Low Byte								
INDF1	, , ,		ddress data n	nemory – valur	of FSR1 not	changed (not	a physical regis	ter)				
POSTINC1							(not a physical					
POSTDEC1 PREINC1							d (not a physica not a physical r					
PLUSW1	Uses content	s of FSR1 to a					not a physical r					
FSR1H	value of FSR	— W Value of	-	-	Indirect Data	Memory Addr	ess Pointer 1, F	ligh Byte				
FSR1L	Indirect Data	Memory Addr	ess Pointer 1 I		D1 -	31-1						
BSR INDF2	Uses content	s of FSR2 to a	ddress data n		Bank Select F of FSR2 not		a physical regis	ter)				
POSTINC2	Uses content	s of FSR2 to a	ddress data n	nemory – value	of FSR2 pos	t-incremented	(not a physical	register)				
POSTDEC2 PREINC2							d (not a physica not a physical r					
PLUSW2	Uses content	s of FSR2 to a					not a physical r					
FSR2H	value of FSR	_ onset by W	_	-	Indirect Data	Memory Addr	ess Pointer 2, H	ligh Byte				
FSR2L	Indirect Data	Memory Addr	ess Pointer 2 I									
STATUS TMR0H	Timer() Regis	ter High Byte		N	OV	Z	DC	С				
TMR0L	Timer0 Regis											
TOCON	TMR00N	T08BIT IRCF2	TOCS IRCF1	TOSE IRCF0	PSA	T0PS2 IOFS	T0PS1 SCS1	T0PS0				
OSCCON HLVDCON	IDLEN VDIRMAG	- IRCF2	IRVST	HLVDEN	OSTS HLVDL3	HLVDL2	HLVDL1	SCS0 HLVDL0				
WDTCON	_	-	-	_	-	-	_	SWDTEN				
RCON TMR1H	IPEN Timer1 Regis	SBOREN <sup>(1)</sup> ster High Byte	_	RI	TO	PD	POR	BOR				
TMR1L	Timer1 Regis											
T1CON	RD16	T1RUN	T1CKPS1	T1CKPS0	T10SCEN	T1SYNC	TMR1CS	TMR10N				
TMR2 PR2	Timer2 Regis Timer2 Perior											
T2CON	_	T2OUTPS3	T2OUTPS2	T20UTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS				
SSPBUF	SSP Receive	Buffer/Transn	nit Register									
SSPADD							Master Mode.					
SSPSTAT	SMP	CKE	D/A	P	S	R/W	UA	BF				
SSPCON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0				
SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN				
ADRESH ADRESL		egister High B egister Low B										
ADCON0	-	_	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON				
ADCON1	— ADFM	_	VCFG1 ACQT2	VCFG0 ACQT1	PCFG3	PCFG2	PCFG1 ADCS1	PCFG0 ADCS0				
ADCON2 CCPR1H		pare/PWM Re			ACQT0	ADCS2	ADCST	ADUSU				
CCPR1L	Capture/Com	pare/PWM Re	gister 1 Low E	Byte								
CCP1CON	P1M1 <sup>(2)</sup>	P1M0 <sup>(2)</sup>	DC1B1									
CCPR2H			DOIDI	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0				
CCPROI		pare/PWM Re	gister 2 High I	Byte	ССР1МЗ	CCP1M2	CCP1M1	CCP1M0				
CCPR2L CCP2CON		npare/PWM Re	gister 2 High I	Byte	CCP1M3	CCP1M2	CCP1M1	CCP1MC				
CCP2CON BAUDCON	Capture/Com — ABDOVF	pare/PWM Re	egister 2 High I egister 2 Low E DC2B1	Byte Byte DC2B0 SCKP	CCP2M3 BRG16	CCP2M2	CCP2M1 WUE	CCP2M0				
CCP2CON BAUDCON PWM1CON	Capture/Com	pare/PWM Re	gister 2 High I	Byte Byte DC2B0	CCP2M3		CCP2M1	CCP2M0				
CCP2CON BAUDCON PWM1CON ECCP1AS CVRCON	Capture/Com  ABDOVF PRSEN ECCPASE CVREN	PDC6 <sup>(2)</sup> ECCPAS2 CVROE	egister 2 High I ggister 2 Low E DC2B1 — PDC5 <sup>(2)</sup> ECCPAS1 CVRR	Byte  Byte  DC2B0  SCKP  PDC4 <sup>(2)</sup> ECCPAS0  CVRSS	CCP2M3 BRG16 PDC3 <sup>(2)</sup> PSSAC1 CVR3	CCP2M2  — PDC2 <sup>(2)</sup> PSSAC0 CVR2	CCP2M1 WUE PDC1 <sup>(2)</sup> PSSBD1 <sup>(2)</sup> CVR1	CCP2M( ABDEN PDC0 <sup>(2)</sup> PSSBD0 <sup>(</sup> CVR0				
CCP2CON BAUDCON PWM1CON ECCP1AS	Capture/Com  ABDOVF PRSEN ECCPASE CVREN C2OUT	PDC6 <sup>(2)</sup> ECCPAS2 CVROE C10UT	egister 2 High I egister 2 Low E DC2B1 — PDC5 <sup>(2)</sup> ECCPAS1	Byte  Byte  DC2B0  SCKP  PDC4(2)  ECCPAS0	CCP2M3 BRG16 PDC3 <sup>(2)</sup> PSSAC1	CCP2M2  — PDC2 <sup>(2)</sup> PSSAC0	CCP2M1 WUE PDC1(2) PSSBD1(2)	CCP2M0 ABDEN PDC0 <sup>(2)</sup> PSSBD0 <sup>(</sup>				
CCP2CON BAUDCON PWM1CON ECCP1AS CVRCON CMCON	Capture/Com  ABDOVF PRSEN ECCPASE CVREN C2OUT	Pare/PWM Re RCIDL PDC6 <sup>(2)</sup> ECCPAS2 CVROE C1OUT	egister 2 High I ggister 2 Low E DC2B1 — PDC5 <sup>(2)</sup> ECCPAS1 CVRR	Byte  Byte  DC2B0  SCKP  PDC4 <sup>(2)</sup> ECCPAS0  CVRSS	CCP2M3 BRG16 PDC3 <sup>(2)</sup> PSSAC1 CVR3	CCP2M2  — PDC2 <sup>(2)</sup> PSSAC0 CVR2	CCP2M1 WUE PDC1 <sup>(2)</sup> PSSBD1 <sup>(2)</sup> CVR1	CCP2M( ABDEN PDC0 <sup>(2)</sup> PSSBD0 <sup>(</sup> CVR0				
ECCP2CON BAUDCON PWM1CON ECCP1AS CVRCON CMCON TMR3H TMR3L T3CON	Capture/Com  ABDOVF PRSEN ECCPASE CVREN C2OUT Timer3 Regis RD16	pare/PWM Re RCIDL PDC6 <sup>(2)</sup> ECCPAS2 CVROE C1OUT ter High Byte tter Low Byte T3CCP2	egister 2 High I egister 2 Low B DC2B1 — PDC5(2) ECCPAS1 CVRR C2INV T3CKPS1	Byte Syte DC280 SCKP PDC4 <sup>(2)</sup> ECCPAS0 CVRSS C1INV	CCP2M3 BRG16 PDC3 <sup>(2)</sup> PSSAC1 CVR3	CCP2M2  — PDC2 <sup>(2)</sup> PSSAC0 CVR2	CCP2M1 WUE PDC1 <sup>(2)</sup> PSSBD1 <sup>(2)</sup> CVR1	CCP2M( ABDEN PDC0 <sup>(2)</sup> PSSBD0 <sup>(</sup> CVR0				
CCP2CON BAUDCON PWM1CON ECCP1AS CVRCON CMCON TMR3H TMR3L T3CON SPBRGH	Capture/Com  ABDOVF PRSEN ECCPASE CVREN C2OUT Timer3 Regis RD16 EUSART Bat	PDRE/PWM Re RCIDL PDC6(2) ECCPAS2 CVROE C1OUT ster High Byte ster Low Byte	gister 2 High I gister 2 Low E DC2B1 — PDC5(2) ECCPAS1 CVRR C2INV T3CKPS1 ator Register I	Byte Syte DC280 SCKP PDC4 <sup>(2)</sup> ECCPAS0 CVRSS C1INV T3CKPS0 High Byte	CCP2M3 BRG16 PDC3 <sup>(2)</sup> PSSAC1 CVR3 CIS	CCP2M2  — PDC2 <sup>(2)</sup> PSSAC0 CVR2 CM2	CCP2M1 WUE PDC1 <sup>(2)</sup> PSSBD1 <sup>(2)</sup> CVR1 CM1	CCP2M0 ABDEN PDC0(2) PSSBD0( CVR0 CM0				
CCP2CON BAUDCON PWM1CON ECCP1AS CVRCON CMCON TMR3H TMR3L T3CON SPBRGH SPBRG RCREG	Capture/Com  ABDOVF PRSEN ECCPASE CVREN C2OUT Timer3 Regis RD16 EUSART Bat EUSART Bat EUSART Ref	pare/PWM Re RCIDL PDC6(2) ECCPAS2 CVROE C10UT ster High Byte trace Low Byte T3CCP2 ud Rate Gener ud Rate Gener ceive Register	rgister 2 High III rgister 2 Low E pocati  — PDCs(2) ECCPAS1 CVRR C2INV  T3CKPS1 ator Register I	Byte Syte DC280 SCKP PDC4 <sup>(2)</sup> ECCPAS0 CVRSS C1INV T3CKPS0 High Byte	CCP2M3 BRG16 PDC3 <sup>(2)</sup> PSSAC1 CVR3 CIS	CCP2M2  — PDC2 <sup>(2)</sup> PSSAC0 CVR2 CM2	CCP2M1 WUE PDC1 <sup>(2)</sup> PSSBD1 <sup>(2)</sup> CVR1 CM1	CCP2M0 ABDEN PDC0(2) PSSBD0( CVR0 CM0				
CCP2CON BAUDCON PWM1CON ECCP1AS CVRCON CMCON TMR3H TMR3L T3CON SPBRGH SPBRG RCREG TXREG	Capture/Com  ABDOVF PRSEN ECCPASE CVREN C2OUT Timer3 Regis RD16 EUSART Bat EUSART Bat EUSART Bat EUSART Bat	pare/PWM Re  RCIDL PDC6 <sup>(2)</sup> ECCPAS2 CVROE C10UT ster High Byte ster Low Byte T3CCP2 ud Rate Gener ud Rate Gener ud Rate Gener ceive Register	igister 2 High in igister 2 Low E DC2B1 — PDC5(2) ECCPAS1 CVR C2INV — T3CKPS1 ator Register I ator Register I	Byte  DC2B0  SCKP PDC4(2)  ECCPAS0  CVRSS  C1INV  T3CKPS0  High Byte  Low Byte	CCP2M3 BRG16 PDC3(P) PSSAC1 CVR3 CIS T3CCP1	CCP2M2 — PDC2 <sup>(2)</sup> PSSAC0 CVR2 CM2 T3SYNC	CCP2M1 WUE PDC1(2) PSSBD1(2) CVR1 CM1 TMR3CS	CCP2M0 ABDEN PDC0(2) PSSBD0( CVR0 CM0				
CCP2CON BAUDCON PWM1CON ECCP1AS CVRCON CMCON TMR3H TMR3H T3CON SPBRGH SPBRG RCREG TXREG TXSTA	Capture/Com  ABDOVF PRSEN ECCPASE CVREN C2OUT Timer3 Regis RD16 EUSART Bat EUSART Bat EUSART Ref	pare/PWM Re RCIDL PDC6(2) ECCPAS2 CVROE C10UT ster High Byte trace Low Byte T3CCP2 ud Rate Gener ud Rate Gener ceive Register	rgister 2 High III rgister 2 Low E pocati  — PDCs(2) ECCPAS1 CVRR C2INV  T3CKPS1 ator Register I	Byte Syte DC280 SCKP PDC4 <sup>(2)</sup> ECCPAS0 CVRSS C1INV T3CKPS0 High Byte	CCP2M3 BRG16 PDC3 <sup>(2)</sup> PSSAC1 CVR3 CIS	CCP2M2  — PDC2 <sup>(2)</sup> PSSAC0 CVR2 CM2	CCP2M1 WUE PDC1 <sup>(2)</sup> PSSBD1 <sup>(2)</sup> CVR1 CM1	CCP2M0 ABDEN PDC0(2) PSSBD0( CVR0 CM0				
CCP2CON BAUDCON PWM1CON ECCP1AS CVRCON CCMCON TMR3H TMR3L T3CON SPBRGH SPBRG TXREG TXREG TXREG TXSTA RCSTA	Capture/Com  ABOVF PRSEN ECCPASE CVREN C20UT Timer3 Regis RD16 EUSART Bat EUSART Bat EUSART Re EUSART Ta CSRC SPEN	pare/PWM Re  — RCIDL PDC6 <sup>[2]</sup> ECCPAS2 CVROE C10UT tet High Byte tet Low Byte T3CCP2 ud Rate Gener ud Rate Gener namit Register namit Register	igister 2 High II gister 2 Low E DC2B1  — DC2B1  — DC2B1  — DC2B1  — CVRR C2INV  T3CKPS1  ator Register I ator Register I TXEN SREN  —	Byte  DC2B0  SCKP  PDC4[2)  ECCPPASO  CVRSS  C1INV  T3CKPS0  High Byte  SYNC	CCP2M3 BRG16 PDC3 <sup>[2]</sup> PSSAC1 CVR3 CIS T3CCP1	CCP2M2  — PDC2 <sup>(2)</sup> PSSAC0 CVR2 CM2  T3SYNC	CCP2M1 WUE PDC1(2) PSSBD1(2) CVR1 CM1 TMR3CS	CCP2M( ABDEN PDC0(2) PSSBD0( CVR0 CM0  TMR3ON				
CCP2CON BAUDCON PWM1CON ECCP1AS CVRCON CMCON CMCON TMR3H TMR3L T3CON SPBRGH RCREG TXREG TXREG TXREG TXREG TXREG TCSTA RCSTA	Capture/Com  ABOVF PRSEN ECCPASE CVREN C20UT Timer3 Regis RD16 EUSART Bat EUSART Bat EUSART Re EUSART Ta CSRC SPEN	pare/PWM Re  RCIDL POC6(2) ECCPAS2 CVROE C/OUT teter High Byte teter Low Byte T3CCP2 dd Rate Gener uch Register Deve Register TX9 RX9 RX9 Ldress Register	igister 2 High II gister 2 Low E DC2B1  — DC2B1  — DC2B1  — DC2B1  — CVRR C2INV  T3CKPS1  ator Register I ator Register I TXEN SREN  —	Byte  DC2B0  SCKP  PDC4[2)  ECCPPASO  CVRSS  C1INV  T3CKPS0  High Byte  SYNC	CCP2M3 BRG16 PDC3 <sup>[2]</sup> PSSAC1 CVR3 CIS T3CCP1	CCP2M2  — PDC2 <sup>(2)</sup> PSSAC0 CVR2 CM2  T3SYNC	CCP2M1 WUE PDC1(8) PSSBD1(9) CVR1 CM1 TMR3CS	CCP2M( ABDEN PDC0(2) PSSBD0( CVR0 CM0  TMR3ON				
CCP2CON BAUDCON PWM1CON ECCP1AS CVRCON CMCON TMR3H TMR3L T3CON SPBRGH RCREG TXREG TXREG TXSTA RCSTA EEADRH EEADRH EEEDATA EECON2	Capture/Com  ABOOVF PRSEN ECCPASE CVREN C2OUT Timer3 Regia RD16 EUSART Bet EUSART Bet EUSART Tet CSRC SPEN EPROM Ad EEPROM Ad EEPROM CO EEPROM CO	pare/PWM Re  RCIDL PDC6(3) ECCPAS2 CVROE C10UT ter High Byte ter Low Byte T3CCP2 Ad Rate Gener ad Rate Gener ceive Register nsmit Register TX9 RX9 Address Register at Register at Register at Register at Register	ingister 2 High in ingister 2 Low E DC2B1  DC2B1  DC2B1  DC2B1  DC2B1  ECCPAS1  CVRR  C2INV  T3CKPS1  ator Register I ator Register I  TXEN  SREN  T	Byte Syte Syte DC280 SCKP PDC4 <sup>[2]</sup> ECCPAS0 CVRSS C1INV  T3CKPS0 High Byte Low Byte  SYNC CREN —	CCP2M3 BRG16 PDC3(2) PSSAC1 CVR3 CIS T3CCP1 SENDB ADDEN	CCP2M2  PDC2(2) PSSAC0 CVR2 CM2  T3SYNC	CCP2M1 WUE PDC1 <sup>(2)</sup> PSSBD1 <sup>(2)</sup> CVR1 CM1 TMR3CS TRMT OERR EEPROM Addr	CCP2MM ABDEN PDC0(2) PSSBD0(1 CVR0) CM0  TMR3ON  TX9D RX9D Register Hi				
CCP2CON BAUDCON PWM1CON ECCP1AS CVRCON CMCON TMR3H TMR3L T3CON SPBRGH SPBRG RCREG TXREG TXREG TXREG TXREA EEADRH EEADR EEEDATA EECON2 EECON1	Capture/Com  ABOOVF PRSEN ECCPASE CVREN C2OUT Timer3 Regis RD16 EUSART Bat EUSART Bat EUSART Tat CSRC SPEN  EEPROM Ad EEPROM Da EEPROM Da	pare/PWM Re  RCIDL PDC6(2) ECCPAS2 CVROE C10UT ster High Byte ster Low Byte T3CCP2  JA Rate Gener JA	ingister 2 High in ingister 2 Low E DC2B1  DC2B1  DC2B1  DC2B1  DC2B1  ECCPAS1  CVRR  C2INV  T3CKPS1  ator Register I ator Register I  TXEN  SREN  T	Byte Byte DC280 SCKP PDC4IS ECCPAS0 CVRSS C1INV  T3CKPS0 High Byte Low Byte  SYNC CREN	CCP2M3 BRG16 PDC3 <sup>[2]</sup> PSSAC1 CVR3 CIS T3CCP1	CCP2M2  — PDC2 <sup>(2)</sup> PSSAC0 CVR2 CM2  T3SYNC	CCP2M1 WUE PDC1(8) PSSBD1(9) CVR1 CM1 TMR3CS	CCP2M( ABDEN PDC0(2) PSSBD0( CVR0 CM0  TMR3ON				
CCP2CON BAUDCON PWM1CON ECCP1AS CVRCON CVRCON CMCON TMR3L T3CON SSPBRGH SSPBRGH SSPBRGH SSPBRG TXREG TXSTA RCSTA READRH EEADR EEEDATA EECON2 EECON1 IPR2	Capture/Com  ABDOVF PRSEN ECCPASE CVPEN C2OUT Timer3 Regis RD16 EUSART Bat EUSART Bat EUSART Tra CSRC SPEN EEPROM Ad EEPROM CO	pare/PWM Re  — CIDL PDC6 <sup>[2]</sup> ECCPAS2 CVROE C10UT teter High Byte teter Low Byte T3CCP2 dd Rate Gener ud Rate Gener TX9 RX9 CHIP CHIP CHIP CMIF	ingister 2 High in ingister 2 Low E DC2B1  DC2B1  DC2B1  DC2B1  DC2B1  ECCPAS1  CVRR  C2INV  T3CKPS1  ator Register I ator Register I  TXEN  SREN  T	Byte Syte Syte Dc280 SCKP PDC4(2) ECCPAS0 CVRSS C1INV  T3CKPS0 High Byte Low Byte  SYNC CREN —  cal register) FREE EEIF	CCP2M3 BRG16 PDC3(2) PSSAC1 CVR3 CIS T3CCP1  SENDB ADDEN — WRERR BCLIP BCLIF	CCP2M2  — PDC2(2) PSSAC0 CVR2  CM2  T3SYNC  BRGH FERR  — WREN HLVDIP HLVDIF	CCP2M1 WUE PDC1 <sup>(2)</sup> PSSBD1 <sup>(2)</sup> CVR1 CM1 TMR3CS TRMT OERR EEPROM Addr	CCP2MC ABDEN PDC06121 PSSBD061 CVR0 CM0 TMR3ON TX9D RX9D Register Hi RD CCP21P CCP21F				
CCP2CON BAUDCON PWM1CON ECCP1AS CVRCON CMCON CMCON CMCON TMR3L T3CON SPBRGH SPBRGH SPBRGH SPBRGR RCREG TXREG TXRET RCSTA RESTA RESTA READR EEADR EECON	Capture/Com  ABDOVF PRSEN ECCPASE CVREN C20UT Timer3 Regie Timer3 Regie Timer3 Regie Timer3 Regie EUSART Bat EUSART Ret EUSART Ret EUSART Tac CSRC SPEN EEPROM Ad EEPROM CO EEPR	pare/PWM Re  RCIDL PDC6f <sup>2</sup> ) ECCPAS2 CVROE C10UT ster High Byte T3CCP2 ad Rate Gener ad Rate Gener ad Rate Gener selve Register TX9 RX9  dress Register ta Register trior Register trior Register CFGS CMIP CMIE	gister 2 High is gister 2 Low E DC2B1 — PDC5(2) ECCPAS1 CVRR C2INV  T3CKPS1 ator Register lator	Byte Syte Syte DC280 DC280 SCKP PDC4(R) ECCPAS0 CVRSS C1INV  T3CKPS0 High Byte Low Byte SYNC CREN — Cal register) FREE EEIP EEIF EEIE	CCP2M3 BRG16 PDC3(P) PSSAC1 CVR3 CIS T3CCP1  SENDB ADDEN — WRERR BCLIP BCLIE	CCP2M2  PDC2(2) PSSAC0 CVR2 CM2  T3SYNC  BRGH FERR  WREN HLVDIP HLVDIE HLVDIE	CCP2M1 WUE PDC1(8) PSSBD1(9) CVR1 CM1 TMR3CS  TRMT OERR EEPROM Addr WR TMR3IP TMR3IE	CCP2MC ABDEN PDC0(2) PSSBD0(1 CVR0 CM0 TMR3ON TX9D RX9D RX9D RC9 CCP2IE CCP2IE CCP2IE				
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CCP2CON BAUDCON BAUDCON PVMTCON ECCP1AS CVRCON CCMCON TMR3H TMR3L T3CON SPBRGH SPBRG TXSTA RCREG TXREG TXSTA EEADR EEADR EECON2 EECON2 EECON2 EECON1 IPR2 PIE2 PIE2 PIE1	Capture/Com  ABDOVF PRSEN ECCPAES CVREN C20UT Timer3 Regie EUSART Bate EUSART Rete EUSART Rete EUSART Tac CSRC SPEN  EEPROM Ad EEPROM CO E	pare/PWM Re  RCIDL PDG6(3) ECCPAS2 CVROE C10UT ster High Byte T3CCP2 d Rate Gener dd Rate Gener dd Rate Gener ceive Register nsmit Register TX9 RX9 Cdress Register chrol R	gjeter 2 High i gjeter 2 Low E DC2B1  — PDC5(2) ECCPAS1 CVRR C2INV T3CKPS1 ator Register ator Register ator Register ator Register i TXEN SREN — 1 2 (not a physic	Byte Syte Syte DC280 DC280 DC280 SCKP PDC4(R) ECCPAS0 CVRSS C1INV  T3CKPS0 High Byte Low Byte  SYNC CREN — FREE EEIP EEIP EEIE TXIP TXIE TXIE	CCP2M3 BRG16 PDC3(P) PSSAC1 CVR3 CIS T3CCP1  SENDB ADDEN — WRERR BCLIP BCLIE BCLIE SSPIP SSPIE	CCP2M2  PDC2(2) PSSAC0 CVR2 CM2  T3SYNC  BRGH FERR  WREN HLVDIP HLVDIE CCP1IE CCP1IE	CCP2M1 WUE PDC1(8) PSSBD1(9) CW1 CW1 CM1 TMR3CS  TRMT OERR EEPROM Addr WR TMR3IP TMR3IP TMR3IE TMR2IP TMR2IP TMR2IE	CCP2MM ABDEN ABDEN PDC0 <sup>12</sup> PSSB00 <sup>1</sup> CM0 CM0  TMR3ON  TX90 Register Hi RD CCP2IP CCP2IP TMR1IPITMR11ET TMR1IPITMR11ET TMR1IPITMR11ET TMR1IPITMR11ET TMR1IPITMR11ET TMR1IPITMR11ET TMR1IPITMR11ET TMR1IPITMR11ET TMR1IPITMR1				
CCP2CON BAUDGON BAUDGON PWMTCON ECCP1AS CVRCON COMCON TMR3H TMR3L T3CON SPBRGH SPBRG RCREG TXREG TXREG TXREG TXSTA EEADRH EEADRH EECON1 EECON1 EEPCCN1	Capture/Com  ABDOVF PRSEN ECCPASE CVFEN C2OUT Timer3 Regis RD16 EUSART Bat EUSART Bat EUSART Tra CSRC SPEN EEPROM Ad EEPROM CO	pare/PWM Re  RCIDL PDC6 <sup>(2)</sup> RCIDL PDC6 <sup>(2)</sup> ECCPAS2 CVROE C10UT teter High Byte teter Low Byte T3CCP2 dr Rate Gener dr Rate Gener dr Rate Gener dr Rate RCIDL RCI	gister 2 High I gister 2 Low E DC2B1  — DC2B1  — PDC5(2) ECCPAS1 CVRR C2INV  T3CKPS1 ator Register I ator Register I TXEN SREN — F C2 (not a physic	Byte Byte Byte Byte Byte Byte Byte Byte	CCP2M3 BRG16 PDC3(2) PSSAC1 CVR3 CIS  T3CCP1  SENDB ADDEN — WRERR BCLIP BCLIF BCLIE SSPIP SSPIF	CCP2M2  PDC2(3) PSSAC0 CVR2  CM2  T3SYNC  BRGH FERR  HUVDIP HLVDIF HLVDIE CCP1IF	CCP2M1 WUE PDC1 <sup>(2)</sup> PSSBD1 <sup>(2)</sup> CVR1 CM1 TMR3CS  TRMT OERR EEPROM Addr WR TMR3IP TMR3IF TMR3IE TMR2IF TMR2IF	CCP2MMP PSSB000 CVR0 CVR0 CVR0 CM0 TMR30h TMR30h CCP2IP CCP2IE CCP2IF TMR1IF1 TMR1IF1 TMR1IF1				
CCP2CON BAUDCON BAUDCON PVMTCON ECCP1AS CVRCON CCMCON TMR3H TMR3L T3CON SPBRGH SPBRG RCREG TXREG TXREG TXREG TXREG EEADR EEEADR EEECON2 EECON2 EECON2 PIR2 PIR2 PIR1 PIR1 PIR1 PIR1 PIR1 PIR1 PIR1 PIR1	Capture/Com  ABDOVF PRSEN ECCPASE CV/REN C20UT Timer3 Regie Timer3 Reg	pare/PWM Re  RCIDL PDG6/3 RCIDL PDG6/3 RCIDL PDG6/3 RCIDL PDG6/3 RCIDL PDG6/3 RCIDL	gister 2 High is gister 2 Low E DC2B1 — PDC5[2] ECCPAS1 CVRR C2INV T3CKPS1 ator Register ator Register ator Register in TXEN SREN — PDC5[2] ECCPAS1 EC	Byte Syte Syte Syte DC280 SCKP PDC4f2) ECCPAS0 CVRSS C1INV  T3CKPS0 High Byte CREN CREN CREN FREE EEIP EEIF EEIF TXIP TXIF TXIE TUN4	CCP2M3 BRG16 PDC3(P) PSSAC1 CVR3 CIS T3CCP1  SENDB ADDEN — WRERR BCLIP BCLIE BCLIE SSPIP SSPIE	CCP2M2  PDC2(2) PSSAC0 CVR2 CM2  T3SYNC  BRGH FERR  HLVDIP HLVDIP HLVDIP CCP1IF CCP1IF TUN2	CCP2M1 WUE PDC1R2 PSSBD1R3 CVR1 CM1 TMR3CS  TRMT OERR EEPROM Addr  WR TMR3IP TMR3IF TMR3IF TMR2IF TM	CCP2MM ABDENN ABDENN PSSB000 CVR0 CVR0 CVR0 TMR3ON TMR3ON Register Hi RD CCP2IP TMR1IP TMR1IF				
CCP2CON BAUDGON BAUDGON PWMTCON ECCP1AS CVPCON CMCON TMR3H TMR3L T3CON SPBRGH SPBRG RCREG TXREG	Capture/Com  ABDOVF PRSEN CCVREN C20UT Timera Regia RD16 EUSART Bat EUSART Bat EUSART Tat EUSART Tran CSRC SPEN  EEPROM Ad EEPROM CO EEP	pare/PWM Re  RCIDL PDG6(3) ECCPAS2 CVROE C10UT ter High Byte ter Low Byte T3CCP2 d Rate Gener delve Register namit Register trick Register namit Register fittol Register (FGS CMIP CMIF ADIF ADIF ADIF ADIF JOHN CORP JOHN CORP DIFFCTOR OF	gister 2 High is gister 2 Low E DC2B1 — PDC5(2) ECCPAS1 CVR C2INV TXEN SREN — C2INV SREN — RCIP RCIP RCIP RCIP RCIP RCIP RCIP RCIP	Byte Syte Syte Syte DC280 SCKP PDC4f2) ECCPAS0 CVRSS C1INV  T3CKPS0 High Byte CREN CREN CREN FREE EEIP EEIF EEIF TXIP TXIF TXIE TUN4	CCP2M3 BRG16 PDC3(P) PSSAC1 CVR3 CIS T3CCP1  SENDB ADDEN — WRERR BCLIP BCLIE BCLIE SSPIP SSPIE	CCP2M2  PDC2(2) PSSAC0 CVR2 CM2  T3SYNC  BRGH FERR  HLVDIP HLVDIP HLVDIP CCP1IF CCP1IF TUN2	CCP2M1 WUE PDC1R2 PSSBD1R3 CVR1 CM1 TMR3CS  TRMT OERR EEPROM Addr  WR TMR3IP TMR3IF TMR3IF TMR2IF TM	CCP2MM ABDENN ABDENN PSSB000 CVR0 CVR0 CVR0 TMR3ON TMR3ON Register Hi RD CCP2IP TMR1IP TMR1IF				
CCP2CON BAUDGON BAUDGON PWMTCON ECCP1AS CVRCON CCMCON TMR3H TMR3L T3CON SPBRGH SPBRG RCREG TXREG TXREG TXREG TXREG TXSTA EECON2 EECON1 IIPR2 PIR2 PIR2 PIR2 PIR1 PIR1 PIR1 PIR1 PIR1 PIR1 PIR1 PIR1	Capture/Com  ABDOVF PRSEN CCVREN C20UT Timera Regia RD16 EUSART Bat EUSART Bat EUSART Tat EUSART Tran CSRC SPEN  EEPROM Ad EEPROM CO EEP	pare/PWM Re  RCIDL PDG6/3 RCIDL PDG6/3 RCIDL PDG6/3 RCIDL PDG6/3 RCIDL PDG6/3 RCIDL	register 2 High II register 2 Low E pocsta pocsta corporation pocsta corporation pocsta corporation pocsta corporation corporation pocsta corporation corporation corporation pocsta corporation corporation pocsta pocsta corporation pocsta p	Byte Syte Syte Syte DC280 SCKP PDC4f2) ECCPAS0 CVRSS C1INV  T3CKPS0 High Byte CREN CREN CREN FREE EEIP EEIF EEIF TXIP TXIF TXIE TUN4	CCP2M3 BRG16 PDC3(2) PSSAC1 CVR3 CIS  T3CCP1  SENDB ADDEN — WRERR BCLIP BCLIF BCLIE SSPIP SSPIF SSPIE TUN3 —	CCP2M2  PDC2(3) PSSAC0 CVR2  CM2  T3SYNC  BRGH FERR  HLVDIP HLVDIF HLVDIE CCP1IE TUN2 TRISE2	CCP2M1 WUE PDC1R2 PSSBD1R3 CVR1 CM1 TMR3CS  TRMT OERR EEPROM Addr  WR TMR3IP TMR3IF TMR3IF TMR2IF TM	CCP2MM ABDENN ABDENN PSSB000 CVR0 CVR0 CVR0 TMR3ON TMR3ON Register Hi RD CCP2IP TMR1IP TMR1IF				
CCP2CON BAUDGON BAUDGON PWMTCON ECCP1AS CVPCON CMCON TMR3H TMR3L T3CON SPBRGH SPBRGR RCREG TXREG TXSTA RCSTA READRH EEADRH EEADRH EEADRH EEFADR EEFADR EEFADR EIFT PIPT PIPT PIPT PIPT TRISE TRISE TRISE TRISE TRISE TRISE	Capture/Com  ABDOVF PRSEN ECCPASE CV/REN C20UT Timer3 Regia Timer3 Regia Timer3 Regia RD16 EUSART Bat EUSART Bat EUSART Tea CSRC SPEN EEPROM Dat EERROM DAT EEPROM DAT EEROM DAT EEPROM DAT EEROM DAT EEPROM DAT EEPROM DAT EEPROM DAT EEROM DAT EEPROM DAT EEROM DAT EEROM DAT EEROM DAT EEPROM DAT EEROM DA	pare/PWM Re  RCIDL PC6(3) RCIDL PC6(3) ECCPAS2 CVROE C10UT tester High Byte T3CCP2 ud Rate Genera da Rate Genera ceive Register nomit Register TX9 RX9  drass Register to FGS MIP CMIE ADIP ADIP ADIP ADIE PLLEN(3) Direction Con Direction Con	register 2 High II register 2 Low E pocsta pocsta corporation pocsta corporation pocsta corporation pocsta corporation corporation pocsta corporation corporation corporation pocsta corporation corporation pocsta pocsta corporation pocsta p	Byte Byte Byte Byte Byte Byte Byte Byte	CCP2M3 BRG16 PDC3(2) PSSAC1 CVR3 CIS  T3CCP1  SENDB ADDEN — WRERR BCLIP BCLIF BCLIE SSPIP SSPIF SSPIE TUN3 —	CCP2M2  —PDC2(2) PSSAC0 CVR2 CM2  T3SYNC  BRGH FERR — WREN HLVDIP HLVDIF HLVDIF CCP1IP CCP1IP CCP1IT TUN2 TRISE2	CCP2M1 WUE PDC1(2) PSSBD1(2) CVR1 CM1  TMR3CS  TRMT OERR EEPROM Addi TMR3IP TMR3IP TMR3IP TMR2IE TMR2ET TMR2ET TMR2ET	CCP2MP PSSB000 CVR0 CVR0 CVR0 TMR301 TMR301 TMR301 TMR301 TMR301 TMR101 TMR101 TMR101 TMR101 TRISE0				
CCP2CON BAUDGON BAUDGON PWMTCON ECCP1AS CVPCON CMCON TMR3H TMR3L T3CON SPBRGH SPBRGH RCREG TXREG TXSTA RCSTA READRH EEADRH EEADRH EEADRH EEADRH EIFT EIFT PIPT PIPT PIPT PIPT TRISE	Capture/Com  ABDOVF PRSEN ECCPAES CV/REN C20UT Timer3 Regie Timer3 Regie Timer3 Regie Timer3 Regie Timer3 Regie Timer3 Regie EUSART Bau EUSART Bau EUSART Refe EUSART Tra CSRC SPEN EEPROM Co EEPROM	pare/PWM Re  RCIDL PDC6f <sup>2</sup> ) RCIDL RCI	gister 2 High is gister 2 Low it pigster 3 Low it pigster 4 Low it pigster	Byte Byte Byte Byte Byte Byte Byte Byte	CCP2M3 BRG16 PDC3(P) PSSAC1 CVR3 CIS T3CCP1  SENDB ADDEN — WRERR BCLIP BCLIE SSPIP SSPIE TUN3 — ster for PORT.	CCP2M2  —PDC2(2) PSSAC0 CVR2 CM2  T3SYNC  BRGH FERR — WREN HLVDIP HLVDIF HLVDIF CCP1IP CCP1IP CCP1IT TUN2 TRISE2	CCP2M1 WUE PDC1(R) PSSBD1(R) CWR1 CM1 CM1 TMR3CS  TRMT OERR EEPROM Addr TMR3IP TMR3IP TMR3IP TMR3IE TMR2IP	CCP2MP PSSB000 CVR0 CVR0 CVR0 TMR301 TMR301 TMR301 TMR301 TMR301 TMR101 TMR101 TMR101 TMR101 TRISE0				
CCP2CON BAUDCON BAUDCON PWM1CON ECCP1AS CVRCON COMCON TMR3H TMR3L T3CON SPBRGH SPBRG RCREG TXREG	Capture/Com  ABDOVF PRSEN ECCPASE CV/REN C20UT Timer3 Regio RD16 EUSART Bet EUSART Bet EUSART Tre CSRC SPEN EEPROM Do EEPROM Do EEPROM Do SCFIP OSCFIP OSCFIP OSCFIP OSCFIE PSIPI(2) INTSRC IBF PORTD Data PORTD Data PORTD Data PORTC Data	pare/PWM Re  RCIDL PDC6(3) ECCPAS2 CVROE C10UT tester High Byte T3CCP2 J4 Rate Gener J5 Rate Gener J6 Rate Gener J7 Rate Gener J	register 2 High II gister 2 Low E DC2B1  DC2B1  DC2B1  CVR C2INV  T3CKPS1 ator Register I ator Register I ator Register I ATXEN SREN  SREN  ROIP ROIP ROIP ROIF ROIE  IBOV trol Register trol Register I T Read and V tr (Read and V	Byte Syte Syte Dc280 SCKP PDC4R SCKP PDC4R ECCPAS0 CVRSS C1INV  T3CKPS0 High Byte Low Byte SYNC CREN CREN CREN CREN TXIF TXIF TXIF TXIE TXIF TXIE TXIR TXIR TXIR TXIR TXIR TXIR TXIR TXIR	CCP2M3 BRG16 PDC3(2) PSSAC1 CVR3 CIS  T3CCP1  SENDB ADDEN — WRERR BCLIP BCLIE SSPIF SSPIE TUN3 — ster for PORT.	CCP2M2  —PDC2(2) PSSAC0 CVR2 CM2  T3SYNC  BRGH FERR — WREN HLVDIP HLVDIF HLVDIF CCP1IP CCP1IP CCP1IT TUN2 TRISE2	CCP2M1 WUE PDC1(2) PSSBD1(2) CVR1 CM1  TMR3CS  TRMT OERR EEPROM Addi TMR3IP TMR3IP TMR3IP TMR2IE TMR2ET TMR2ET TMR2ET	CCP2MP PSSB000 CVR0 CVR0 CVR0 TMR301 TMR301 TMR301 TMR301 TMR301 TMR101 TMR101 TMR101 TMR101 TRISE0				
CCP2CON BAUDCON BAUDCON PWMTCON ECCP1AS CVRCON CCMCON TMR3H TMR3L T3CON SPBRGH SPBRG RCREG TXREG	Capture/Com  ABDOVF PRSEN ECCPAES CVFEN C20UT Timer3 Regie Timer3 Regi	pare/PWM Re  RCIDL PDC6(3) ECCPAS2 CVROE C10UT tester High Byte T3CCP2 J4 Rate Gener J5 Rate Gener J6 Rate Gener J7 Rate Gener J	gister 2 High is gister 2 Low E DC2B1 — PDC5(2) ECCPAS1 CVRR C2INV T3CKPS1 ator Register ator Register ator Register ator Register in TXEN SREN — TXEN SREN — STATE STAT	Byte Syte Syte Syte DC280 SCKP PDC4f2) SCKP PDC4f2) ECCPAS0 CVRSS C1INV  T3CKPS0 High Byte Low Byte SYNC CREN — CREN — CREN — FREE EEIP EEIF EEIF TXIP TXIE TUN4 PSPMODE	CCP2M3 BRG16 PDC3(P) PSSAC1 CVR3 CIS  T3CCP1  SENDB ADDEN — WRERR BCLIP BCLIE SSPIP BCLIE SSPIP SSPIE TUN3 — ster for PORT. — atch)	CCP2M2  PDC2(2) PSSAC0 CVR2 CM2  T3SYNC  BRGH FERR  HLVDIP HLVDIP HLVDIE CCP1IP CCP1IP TUN2 TRISE2  A PORTE Data (Read and W	CCP2M1 WUE PDC1(P) PSSBD1(P) CWR1 CWR1 CM1 TMR3CS  TRMT OERR EEPROM Addr WR TMR3IP TMR3IP TMR3IP TMR2IP TMR	CCP2MP PSSB000 CVR0 CVR0 CVR0 TMR301 TMR301 TMR301 TMR301 TMR301 TMR101 TMR101 TMR101 TMR101 TRISE0				
CCP2CON BAUDGON BAUDGON PWM1CON ECCP1AS CVRCON COMCON TMR3H TMR3L T3CON SPBRGH SPBRG RCREG TXREG	Capture/Com  ABDOVF PRSEN ECCPASE CV/REN C20UT Timer3 Regia RD16 EUSART Bot EUSART Bot EUSART Tre CSPEN EEPROM Do EE	pare/PWM Re  RCIDL PDC6(3) ECCPAS2 CVROE C10UT tester High Byte T3CCP2 Ad Rate Gener between High Byte T3CCP2 AG Rate Gener Celve Register nomit Register CFGS CMIP CMIE ADIP ADIP ADIP ADIP ADIP ADIP ADIP ADIP	gister 2 High I gister 2 Low E DC2B1  PDC5[2] ECCPAS1 CVR C2INV T3CKPS1 ator Register I ator Register I ator Register I TXEN SREN  RCIP RCIP RCIP RCIP RCIP RCIP RCIP RCI	Byte Syte Syte DC280 SCKP PDC4R SCKP PDC4R ECCPAS0 CVRSS C1INV  T3CKPS0 High Byte Low Byte SYNC CREN CREN CREN TXIF TXIF TXIF TXIF TXIE TUN4 PSPMODE	CCP2M3 BRG16 PDC3(2) PSSAC1 CVR3 CIS  T3CCP1  SENDB ADDEN — WRERR BCLIP BCLIF BCLIE SSPIF SSPIE TUN3 — atch) atch) atch) atch) RE3(4)	CCP2M2  PDC2(2) PSSAC0 CVR2 CM2  T3SYNC  BRGH FERR  HLYDIP HLVDIF HLVDIF HLVDIF CCP1IF CCP1IF CCP1IE TUN2 TRISE2  A PORTE Data L RE2(2)	CCP2M1 WUE PDC1(2) PSSBD1(2) CVR1 CM1 TMR3CS  TRMT OERR EEPROM Addi TMR3IP TMR3IP TMR3IP TMR2IE TMR2E1 TMR2E1 TMR2E1 CM1 TMR2E1 TMR2IP	CCP2MP ABDENN PDC0/II PSSB00/I PSSB00/I CVR0 CVR0 TMR3OH TMR3OH TMR3OH TMR3OH TMR1F TMR1IF TM				
CCP2CON BAUDCON PWM1CON ECCP1AS CVRCON CMCON TMR3H TMR3L T3CON SPBRGH SPBRG RCREG	Capture/Com  ABDOVF PRSEN ECCPAES CVFEN C20UT Timer3 Regie Timer3 Regi	pare/PWM Re  RCIDL PDC6(3) ECCPAS2 CVROE C10UT ster High Byte ter Low Byte ter Low Byte T3CCP2 d Rate Gener dd Rate Gener dd Rate Gener ceive Register namin Register TX9 RX9  drates Register nor Register nor Register nor Register nor Register DF GMIP CMIP ADIP ADIP ADIE Direction Con Direction C	gister 2 High is gister 2 Low E DC2B1 — PDC5(2) ECCPAS1 CVRR C2INV T3CKPS1 ator Register ator Register ator Register ator Register in TXEN SREN — TXEN SREN — STATE STAT	Byte Syte Syte DC280 DC280 DC280 SCKP PDC4(P) ECCPAS0 CVRSS C1INV  T3CKPS0 High Byte Low Byte SYNC CREN — SYNC CREN — FREE EEIP EEIF TXIP TXIE TUN4 PSPMODE  n Control Regi	CCP2M3 BRG16 PDC3(P) PSSAC1 CVR3 CIS  T3CCP1  SENDB ADDEN — WRERR BCLIP BCLIF BCLIF BCLIF SSPIF SSPIF TUN3 — ster for PORT. — atch) atch) atch) (Read and W	CCP2M2  PDC2(2) PSSAC0 CVR2 CM2  T3SYNC  BRGH FERR HLVDIP HLVDIP HLVDIF HLVDIF CCP1IF	CCP2M1 WUE PDC1(2) PSSBD1(2) CVR1 CM1 TMR3CS  TRMT OERR EEPROM Addr WR TMR3IP TMR3IF TMR2IF TMR2IE TMR2ET TMR2IE T	CCP2MP ABDEN ABDEN PDCGG PSSB000 CVR0 CVR0 CVR0 TMR3ON TMR3ON Register Hi RD CCP2IP TMR1IP TMR1ET TMR1ESE0				

18F									
Mnemo		Description	Cycles	$\vdash$	-Bit Ins	truction		Status Affected	Notes
				MSb			LSb	Affected	
		OPERATIONS	la .	1				0.00.7.00	14.0
ADDWF ADDWFC	f, d, a f. d. a	Add WREG and f Add WREG and CARRY bit to f	1	0010	01da0 0da	ffff	ffff	C, DC, Z, OV, N C, DC, Z, OV, N	1, 2
ANDWF	f, d, a	AND WREG with f	1	0001		ffff	ffff	Z, N	1,2
CLRF	f, a	Clear f	1	0110		ffff	ffff	Z	2
COMF	f, d, a f, a	Complement f Compare f with WREG, skip =	1 1 (2 or 3)	0001	11da 001a	ffff	ffff	Z, N None	1, 2 4
CPFSGT	f, a	Compare f with WREG, skip >	1 (2 or 3)	0110			ffff	None	4
CPFSLT	f, a	Compare f with WREG, skip <	1 (2 or 3)	1		ffff	ffff	None	1, 2
DECF DECFSZ	f, d, a f. d. a	Decrement f Decrement f, Skip if 0	1 1 (2 or 3)	0000		ffff	ffff	C, DC, Z, OV, N None	1, 2, 3, 4 1, 2, 3, 4
DCFSNZ	f, d, a	Decrement f, Skip if Not 0	1 (2 or 3)		11da	ffff	ffff	None	1, 2
INCF	f, d, a	Increment f	1 (2 2)	0010		ffff	ffff	C, DC, Z, OV, N	1, 2, 3, 4
INCFSZ	f, d, a f, d, a	Increment f, Skip if 0 Increment f, Skip if Not 0	1 (2 or 3) 1 (2 or 3)			ffff	ffff	None None	1, 2
IORWF	f, d, a	Inclusive OR WREG with f	1 '	0001	00da	ffff	ffff	Z, N	1, 2
MOVE	f, d, a	Move f (acures) to 1 at word	1	0101				Z, N	1
MOVFF	f <sub>s</sub> , f <sub>d</sub>	Move f <sub>s</sub> (source) to 1st word f <sub>d</sub> (destination) 2nd word	2	1111		ffff	ffff	None	
MOVWF	f, a	Move WREG to f	1	0110		ffff	ffff	None	
MULWF	f, a	Multiply WREG with f	1	0000		ffff	ffff	None	1, 2
NEGF RLCF	f,a f,d,a	Negate f Rotate Left f through Carry	1	0110		ffff	ffff	C, DC, Z, OV, N C, Z, N	1, 2
RLNCF	f, d, a	Rotate Left f (No Carry)	1	0100		ffff	ffff		1.,-
RRCF	f, d, a	Rotate Right f through Carry	1	0011					
RRNCF SETF	f, d, a f, a	Rotate Right f (No Carry) Set f	1	0100		ffff	ffff	Z, N None	1, 2
SUBFWB	f, d, a	Subtract f from WREG with	1	0101		ffff	ffff	C, DC, Z, OV, N	.,.
OLIDAYE		borrow							1,
SUBWF SUBWFB	f, d, a f, d, a	Subtract WREG from f Subtract WREG from f with	1	0101 0101	11da 10da	ffff ffff	ffff ffff	C, DC, Z, OV, N C, DC, Z, OV, N	1, 2
SWAPF	fd-	borrow Swap pibbles in f	1	0000	202			None	
TSTFSZ	f, d, a f, a	Swap nibbles in f Test f, skip if 0	1 (2 or 3)	0011	10da 011a	ffff	ffff	None None	1, 2
XORWF	f, d, a	Exclusive OR WREG with f	1	0001	10da	ffff	ffff	Z, N	"-
BIT-ORIEN	ITED OP	ERATIONS .							
BCF	f, b, a	Bit Clear f	1	1001	bbba	ffff	ffff	None	1, 2
BSF BTFSC		Bit Set f	1 1 (2 or 3)	1000	bbba bbba	ffff	ffff ffff	None None	1, 2 3, 4
BTFSS	f, b, a f, b, a	Bit Test f, Skip if Clear Bit Test f, Skip if Set	1 (2 or 3)	1011 1010	bbba	ffff	ffff	None	3, 4
BTG		Bit Toggle f	1 '	0111	bbba	ffff	ffff	None	1, 2
CONTROL	OPERA	TIONS							
BC BN	n	Branch if Carry	1(2)	1110	0010	nnnn	nnnn	None	
BNC	n n	Branch if Negative Branch if Not Carry	1 (2) 1 (2)	1110 1110	0110 0011	nnnn nnnn	nnnn nnnn	None None	
BNN	n	Branch if Not Negative	1 (2)	1110	0111	nnnn	nnnn	None	
BNOV	n	Branch if Not Overflow	1 (2)	1110	0101	nnnn	nnnn	None	
BNZ BOV	n n	Branch if Not Zero Branch if Overflow	1 (2) 1 (2)	1110	0001	nnnn nnnn	nnnn nnnn	None None	
BRA	n	Branch Unconditionally	2	1101	0nnn	nnnn	nnnn	None	
BZ	n	Branch if Zero	1 (2)	1110	0000	nnnn	nnnn	None None	
CALL	n, s	Call subroutine 1st word 2nd word	2	1111	110s kkkk	kkkk kkkk	kkkk kkkk	None	
CLRWDT	_	Clear Watchdog Timer	1	0000	0000	0000	0100	TO, PD	
DAW	_	Decimal Adjust WREG Go to address 1st word	1	0000	0000	0000	0111	C	
GOTO	n	Go to address 1st word 2nd word	2	1110 1111	1111 kkkk	kkkk kkkk	kkkk kkkk	None	
NOP	_	No Operation	1	0000	0000	0000	0000	None	
NOP	_	No Operation	1	1111	XXXX	XXXX		None	4
POP	_	Pop top of return stack (TOS) Push top of return stack (TOS)	1	0000	0000	0000	0110 0101	None None	
RCALL	n	Relative Call	2	1101	1nnn	nnnn	nnnn	None	
RESET RETFIE	s	Software device Reset Return from interrupt enable	1	0000	0000	1111 0001	1111 000s	All GIE/GIEH,	
KEILE	5	riverum mom interrupt enable	_	0000	0000	0001	0008	PEIE/GIEL	
RETLW	k	Return with literal in WREG	2	0000	1100	kkkk	kkkk	None	
RETURN SLEEP	s	Return from Subroutine Go into Standby mode	2	0000	0000	0001	001 <i>s</i> 0011	None TO, PD	
LITERAL C	DEDATI		1.	0000	5500	5500	0011	. 5, 1 5	
ADDLW	k	Add literal and WREG	1	0000	1111	kkkk	kkkk	C, DC, Z, OV, N	
ANDLW	k	AND literal with WREG	1	0000	1011	kkkk	kkkk	Z, N	
IORLW	k	Inclusive OR literal with WREG	1	0000	1001	kkkk	kkkk	Z, N	
LFSR	f, k	Move literal (12-bit) 2nd word to FSR(f) 1st word	2	1110		00ff kkkk	kkkk kkkk	None	
MOVLB	k	Move literal to BSR<3:0>	1	0000	0001	0000	kkkk	None	
MOVLW	k	Move literal to WREG	1	0000	1110	kkkk	kkkk	None	
RETLW	k k	Multiply literal with WREG Return with literal in WREG	1		1101	kkkk		None None	
SUBLW	k k	Subtract WREG from literal	1	0000	1100	kkkk kkkk	kkkk kkkk	C, DC, Z, OV, N	
XORLW	k	Exclusive OR literal with WREG	1	0000	1010	kkkk	kkkk	Z, N	
	IORY ↔	PROGRAM MEMORY OPERATION							
TBLRD*		Table Read	2	0000	0000	0000	1000	None	
TBLRD*+ TBLRD*-		Table Read with post-increment Table Read with post-decrement		0000	0000	0000	1001 1010	None None	
TBLRD+*		Table Read with pre-increment		0000	0000	0000	1011	None	
TBLWT*		Table Write	2	0000	0000	0000	1100	None	
TBLWT*+ TBLWT*-		Table Write with post-increment Table Write with post-decrement		0000	0000	0000	1101 1110	None None	
TBLWT+*		Table Write with pre-increment		0000	0000	0000	1111	None	